AD-A161 928 FUNCTIONAL TESTING OF LSI/VLSI BASED SYSTEMS WITH MEASURE OF FAULT COVERAGE(U) STATE UNIV OF NEW YORK AT ALBANY RESEARCH FOUNDATION S Y SU 08 FEB 83 1/1

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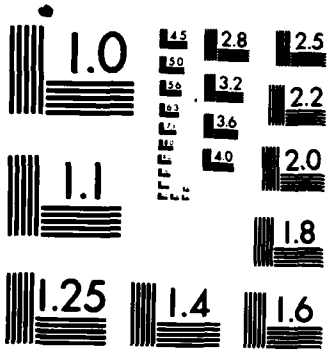

SCIENTIFIC AND TECHNICAL REPORT

THIRD QUARTERLY STATUS REPORT

prepared by

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A. Contractor's name and address:

The Research Foundation of
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C. Date of Report - February 8, 1983

D. Title: The Third Quarterly Report for the project "Functional Testing of LSI/VLSI Based Systems with Measure of Fault Coverage"

E. Period Covered: October 28, 1982 to January 27, 1983

F. Description of Progress:

1) CURRENT RESULTS

Microprocessors are widely used in modern digital systems. To ensure the reliable operations of microprocessors, it is important to have these devices tested before their usage.

This quarter we devote our research effort to develop a simplified algorithm for testing microprocessors.

Thatte and Abraham [1, 2] have proposed a graph model for microprocessor, and based on the model, they develop some initial results in the area of testing microprocessors. However, in their method, not all information available to the microprocessor users are utilized. One of the most important reasons for making microprocessor testing difficult is the

detailed hardward implementation of the microprocessors is unknown to the users in most cases. Therefore, it is important to maximize the use of information obtained from microprocessor manuals and application notes or data sheets. Almost all microprocessor manufacturers provide a reasonable amount of timing and control information about their products, for example, instruction execution time (in terms of the number of clock cycles), READ and WRITE signals, and so forth. We are using this information to simplify the test generation.

As is evident from the previous work of different researchers, the most complex and time consuming task of testing a microprocessor is detecting instruction decoding faults. We, therefore, concentrate on reducing the complexity of test set for detecting faults in instruction decoding function.

The key idea is that we divide all instructions into different partitions using the timing and control information. The new objective, then, is to test instructions in different partitions. Thus a larger problem is solved using the "divide and conquer" strategy by solving general smaller sub-problems.

In the attached paper, we presents a number of algorithms to test the instruction decoding function of microprocessors based on some timing and control information available to users. Keywords: Register Transfer Language, digital networks

In the development of our first algorithm, we divide all instructions into different partitions using the information on instruction execution time. For the second algorithm, we make use of READ and WRITE signals. In this scheme, each instruction is associated with an ordered READ-WRITE sequence. This association is then used to divide the set of all instructions into different partitions. The third one is the mixture of both the above

algorithms to further subdivide the instructions for obtaining a better result.

We establish the order of complexity of the algorithms proposed in the attached paper. As an example, the test complexity for the Intel 8080 is computed and the results are compared with a known algorithm. Our algorithms can reduce the test program size by about 60%.

We also considered other microprocessors, e.g. Intel 8085, 8086, Motorola 6800, Z80, etc., and found that our partitioning methods are applicable to these microprocessors.

Finally, we outlined some strategies to test a microprocessor completely.

The algorithms given in the attached paper are simple, easy to use and efficient. In our treatment, we have used only the information which is common to all microprocessors, thus for any given microprocessor the actual complexity of the tests is likely to be even less then the complexity determined in this paper.

2) MODELING USING REGISTER TRANSFER LANGUAGE

In view of the fact that the knowledge of microprocessor internal circuit (logic level or otherwise) is preparatory information and is normally not available to the users, it is desired to test microprocessors functionally. Here, "functional testing" means we do know the functional behavior of a microprocessor. This includes the set of instructions, input/output behaviour and to a certain degree internal behaviour. Often some knowledge about the architecture and internal registers is also available. For our modeling (behavioural model) we describe a microprocessor using an RTL (Register Transfer Language) description. We choose the RTL language of Min and Su [3]. An RTL statement is as follows:

$$k: \quad (T,C) \quad R_d \leftarrow f(R_{s_1}, R_{s_2}, \ldots, R_{s_p}), \quad \rightarrow n$$

where K: label
(T,C) Timing and Condition
R_d Destination Register
f function
R_{s_i} Source Register
$\rightarrow n$ Jump to label n

With this description of a microprocessor, the objective of testing is to verify RTL description of the behaviour of a microprocessor.

Our RTL model proposed overcomes the problems generated by the inadequacy of the existing model [2,4,5] and has the following properties.

(i) It is a behavioural description of a microprocessor, thus we need not know the gate level realization of a microprocessor.

(ii) It can make use of the architectural information if such information is available. In the absence of such information, one may use a most general description, though it will complicate the testing problem.

(iii) Fault classes are naturally defined and certain fault equivalencies can be established.

(iv) In many fault classes, fault enumerations is possible. In RTL model, the detection of label and jump faults will detect partial execution of instruction faults as well, which are difficult if one uses Thattle and Abraham's [2] model. Verification of RTL implies testing of all instructions.

3) FUTURE WORK

We plan to use the RTL to describe the behavior of digital networks and to help generate test patterns for testing the networks. We shall

explore the bit-oriented testing as proposed by Min and Su [3] for devices other than microprocessors.

The second approach is instruction oriented testing which is suitable for microprocessor testing. We shall start by finding the relationships, including equivalence relation, among various faults in the RTL statements.

G. Spending

Current quarter actual cost: $18,378.63

Cumulative cost to date: $36,796.79

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